Course Type	Course Code	Name of Course	L	T	P	Credit
DE	NECD524	Low Power VLSI	3	0	0	3

Course Objective

This course deals with the design issues of low power circuits in digital perspective. In this course, MOS transistor modelling is emphasized for low power applications. After completing this course the students would have thorough knowledge of modelling of various MOS parameters and SPICE simulation for low power applications, correlation analysis in DSP systems, Monte Carlo simulation and low power memory design.

Learning Outcomes

Upon successful completion of this course, students will be able to:

- analyze the need for low power VLSI circuits
- understand dynamic and static power dissipation and factors affecting them
- recognize role of simulation possible at various levels of design
- define relationship of probability while calculating power dissipation of circuits
- apply Power reduction techniques possible at circuit, logic level
- analyze Clock as a major source of power dissipation and distinguish various methods to reduce it.

Unit No.	Topics to be Covered	Lecture Hours	Learning Outcome
1	Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.	6	Acquire an understanding of the fundamental concepts of Low Power VLSI design.
2	Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation. Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.	9	Understand how to do various types of Power analysis techniques.
3	Low Power Circuits: Transistor and gate sizing, network restructuring and Reorganization. Special Flip Flops & Latches design, high capacitance nodes, low power digital cells library. Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.	9	Develop the skill to design various Low power VLSI system building blocks.
4	Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components.	9	Develop the skill to design Low power architecture and systems.
5	Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network. Special Techniques: Power Reduction in Clock networks, CMOS Floating Node, Low Power Bus Delay balancing, and Low Power Techniques for SRAM.	9	Develop the skill to design Low power clock distribution schemes.
	Total	**42**	

Text Books:

1. G. K.Yeap, Farid N. Najm, "Low Power VLSI design and technology", World Scientific Publishing, 1996.

2. Gary K.Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Press, 1998.
3. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design", Wiley, 2009.

Reference Books:

1. A. P. Chandrakasan, R. W. Broderson, "Low Power Digital VLSI Design", IEEE Press, 1998.
2. Jan M. Rabaey, Massoud Pedram, "Low power Design methodologies", Kluwer Academic Press, 1996.
3. Michael Keating, David Flynn "Low Power Methodology Manual for System On-Chip Design", Springer Publication 2007.